

FIG.1

100

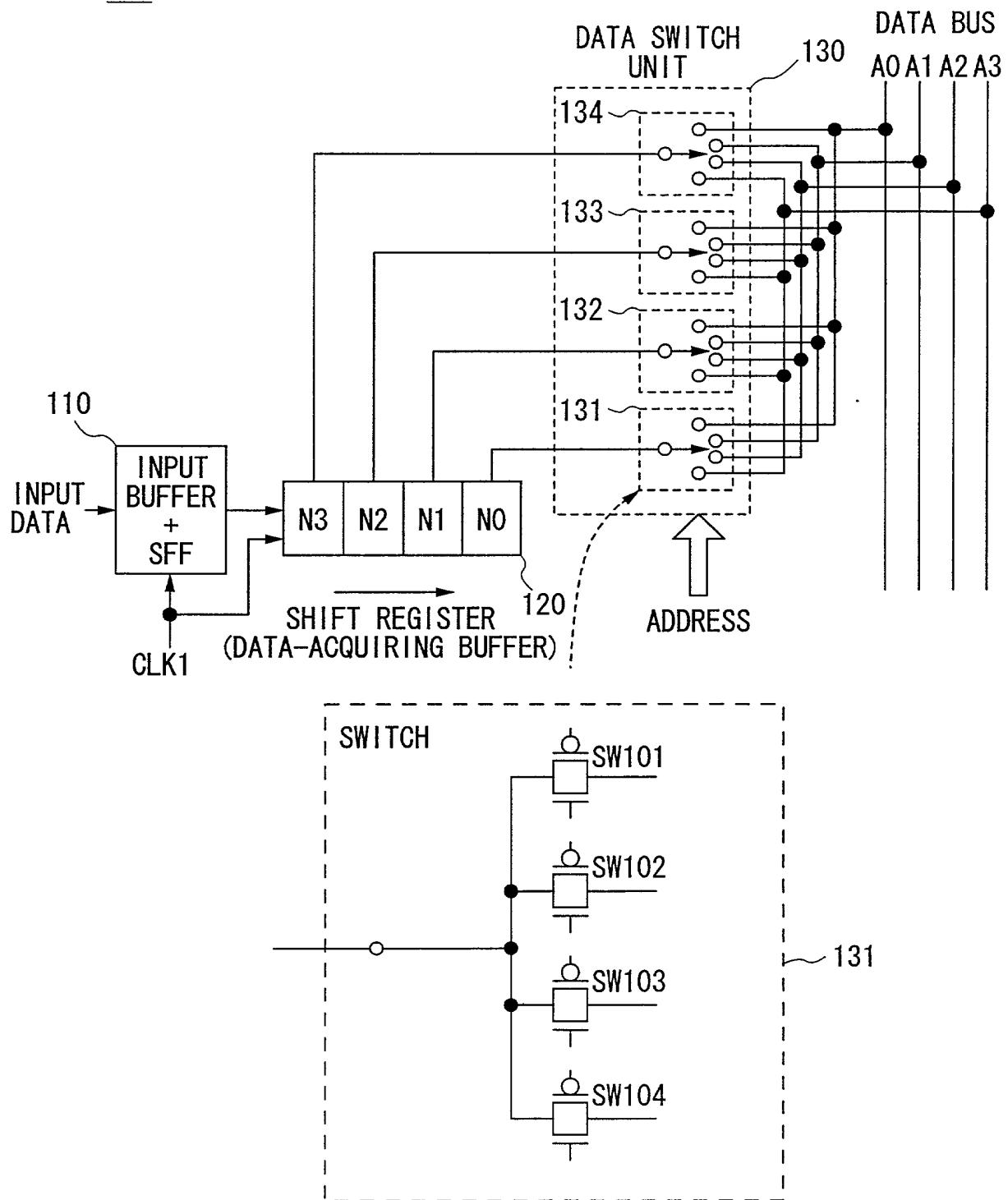


FIG.2A

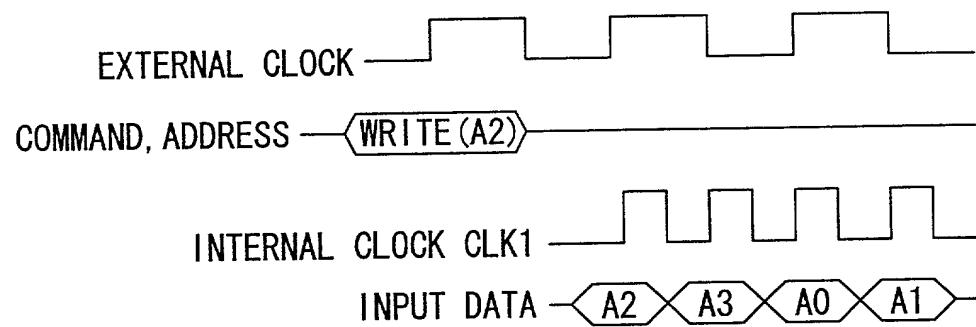


FIG.2B

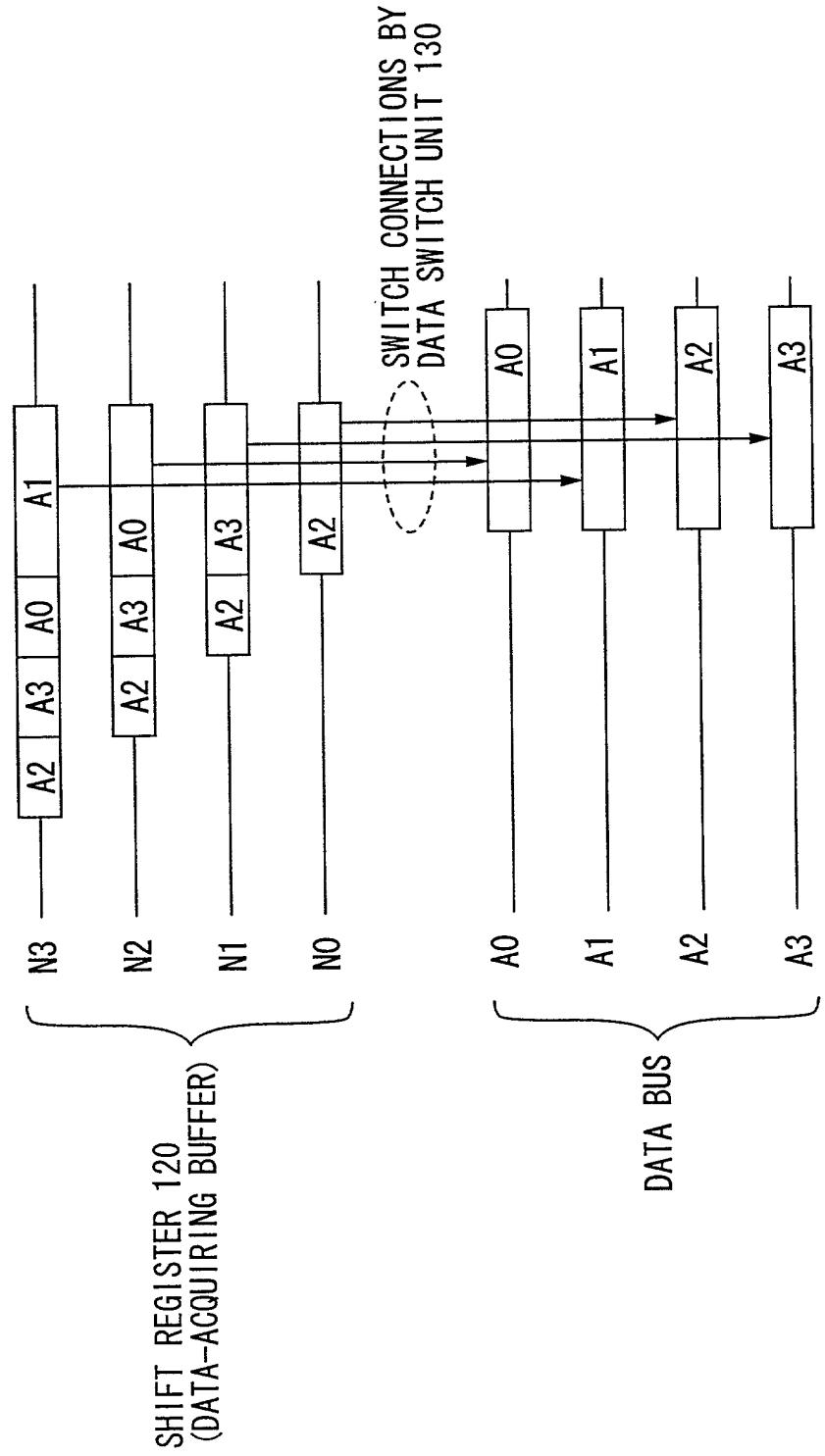


FIG.3

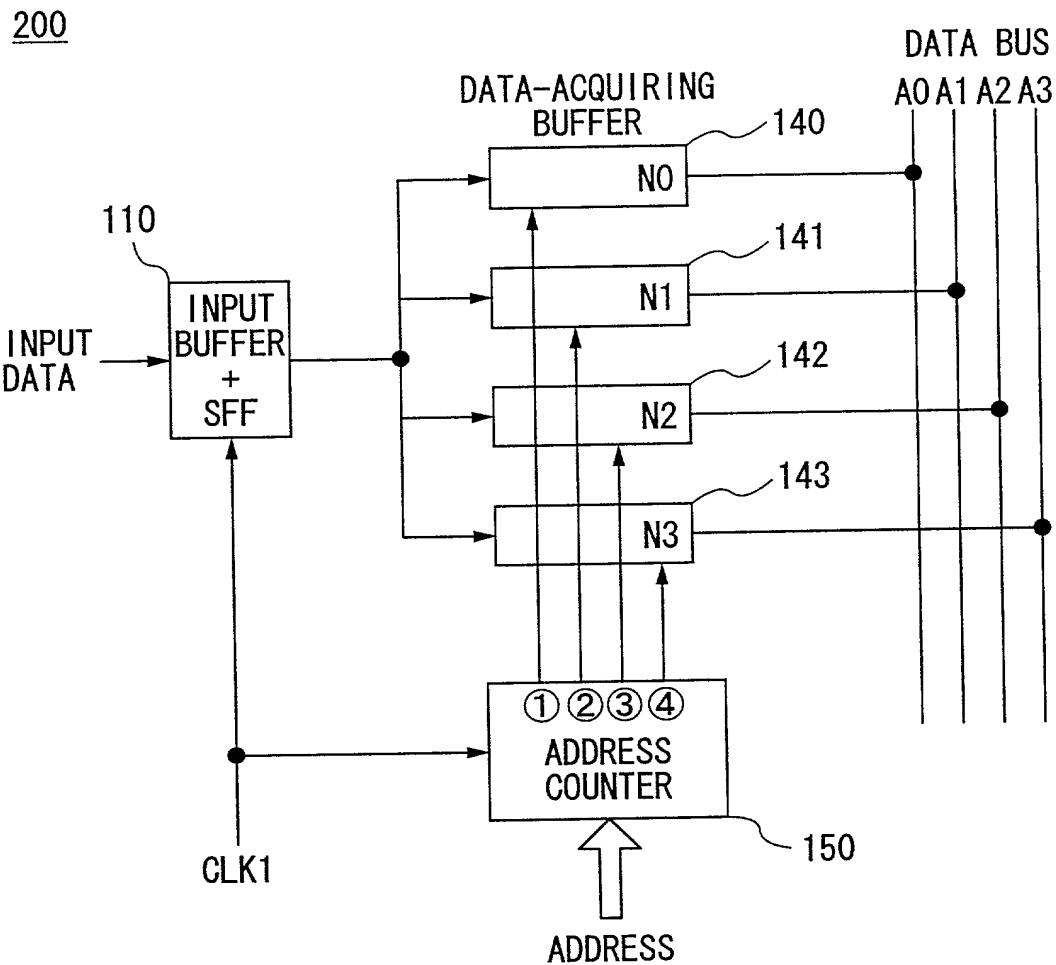


FIG.4A

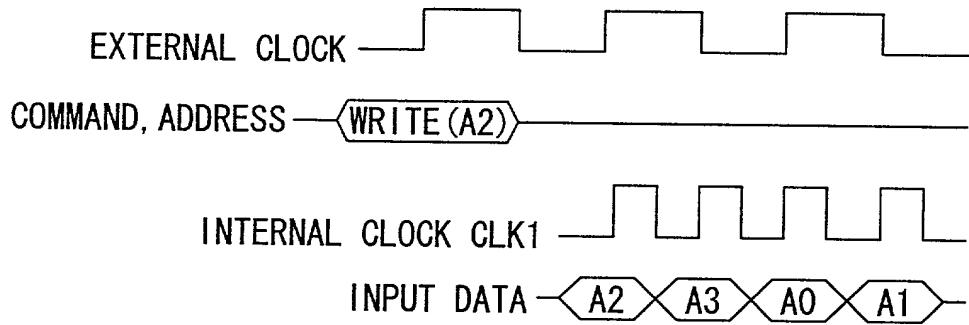


FIG.4B

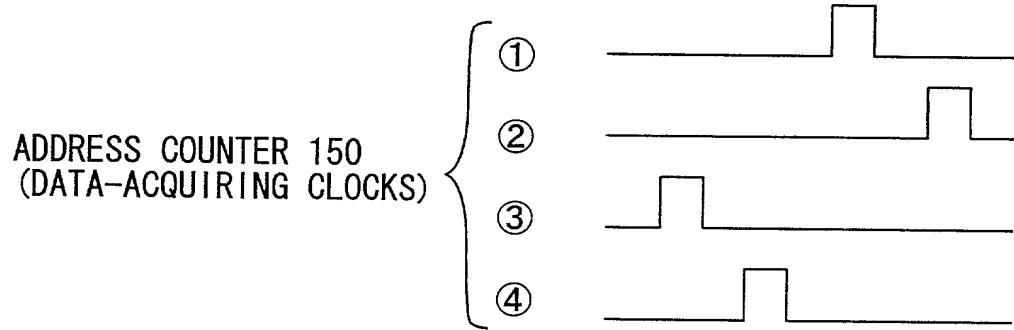


FIG.4C

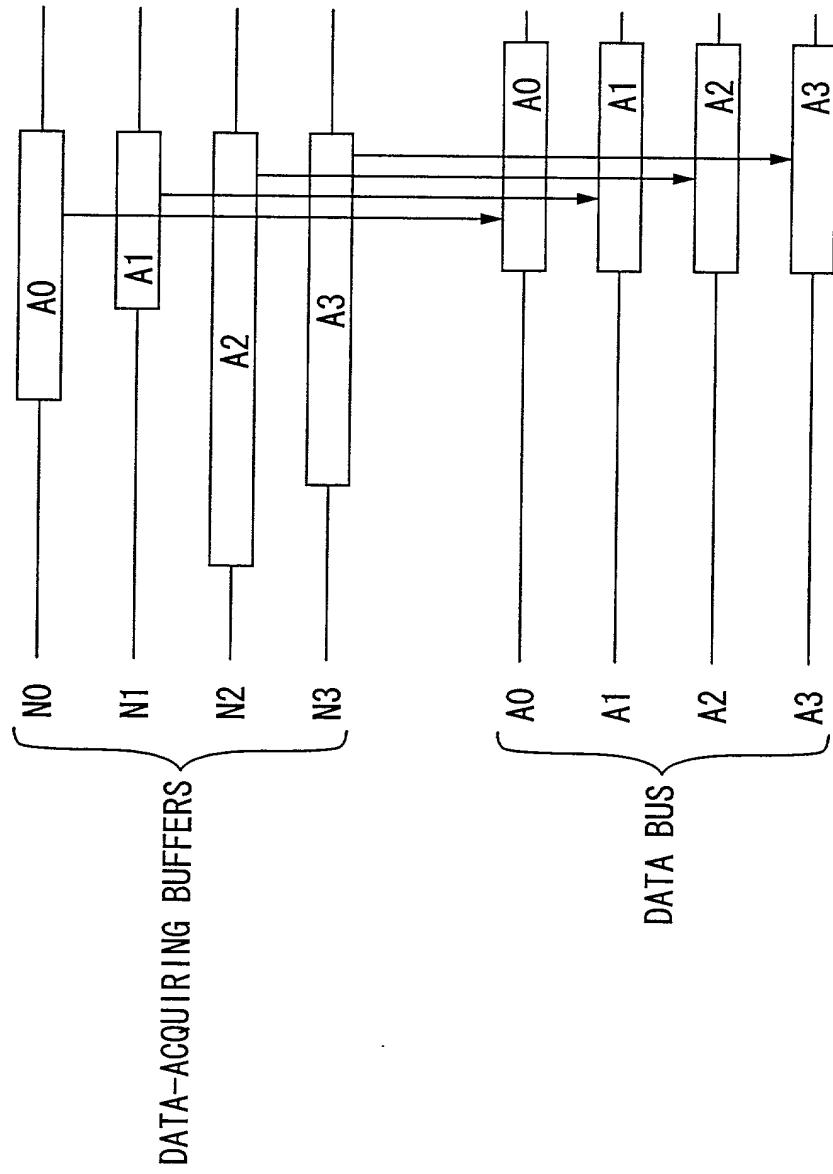


FIG.5

1

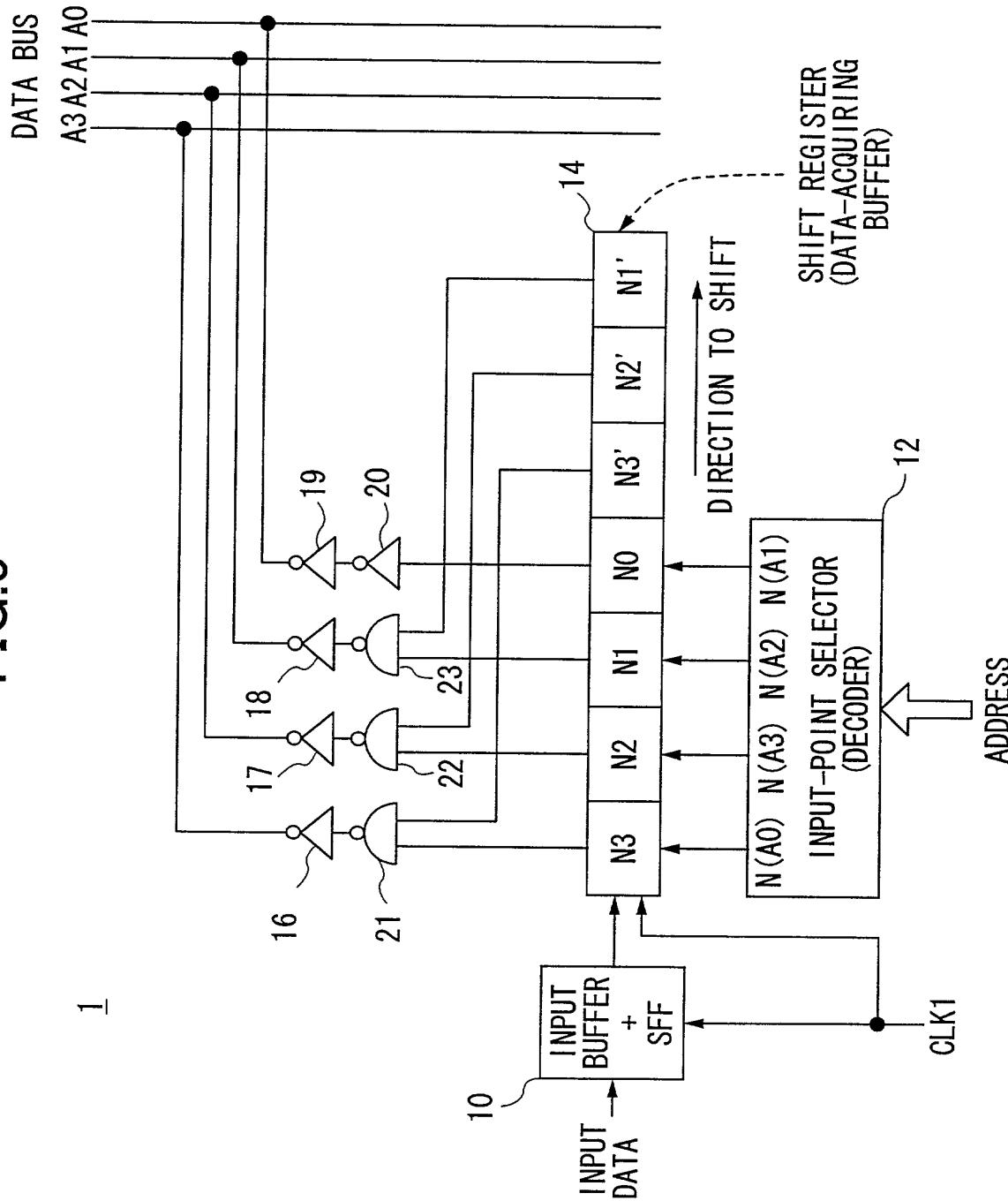


FIG.6A

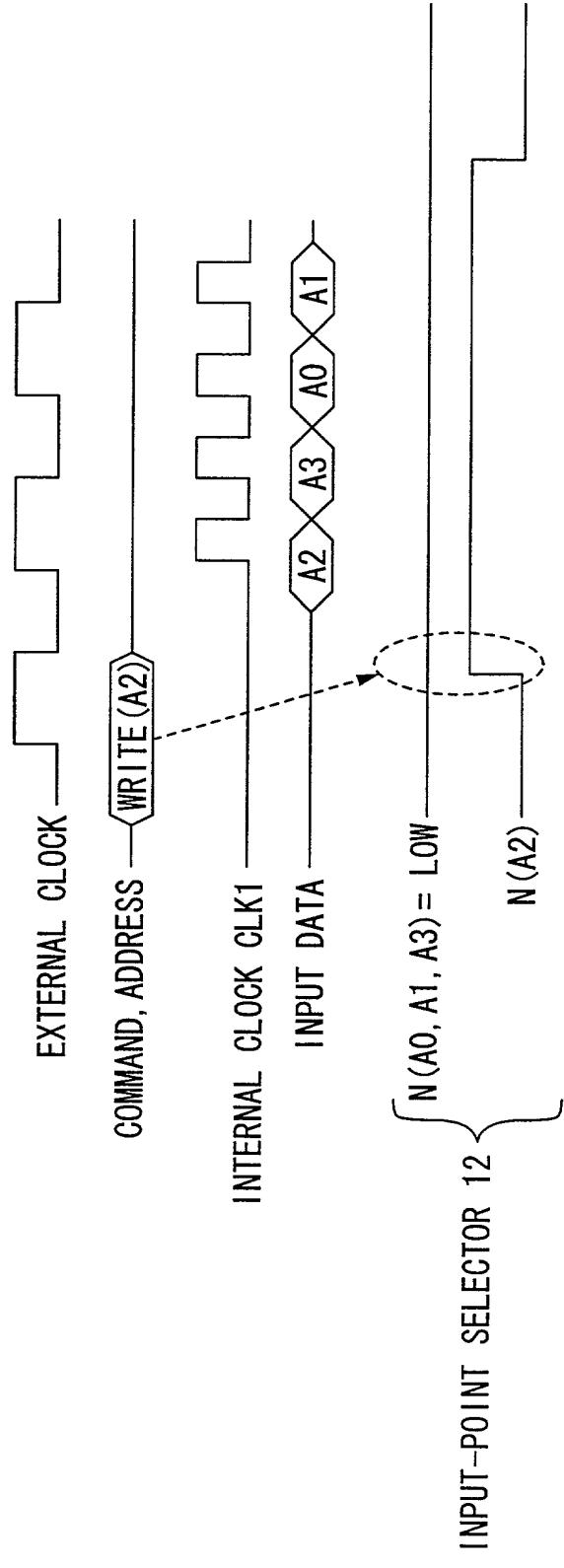


FIG.6B

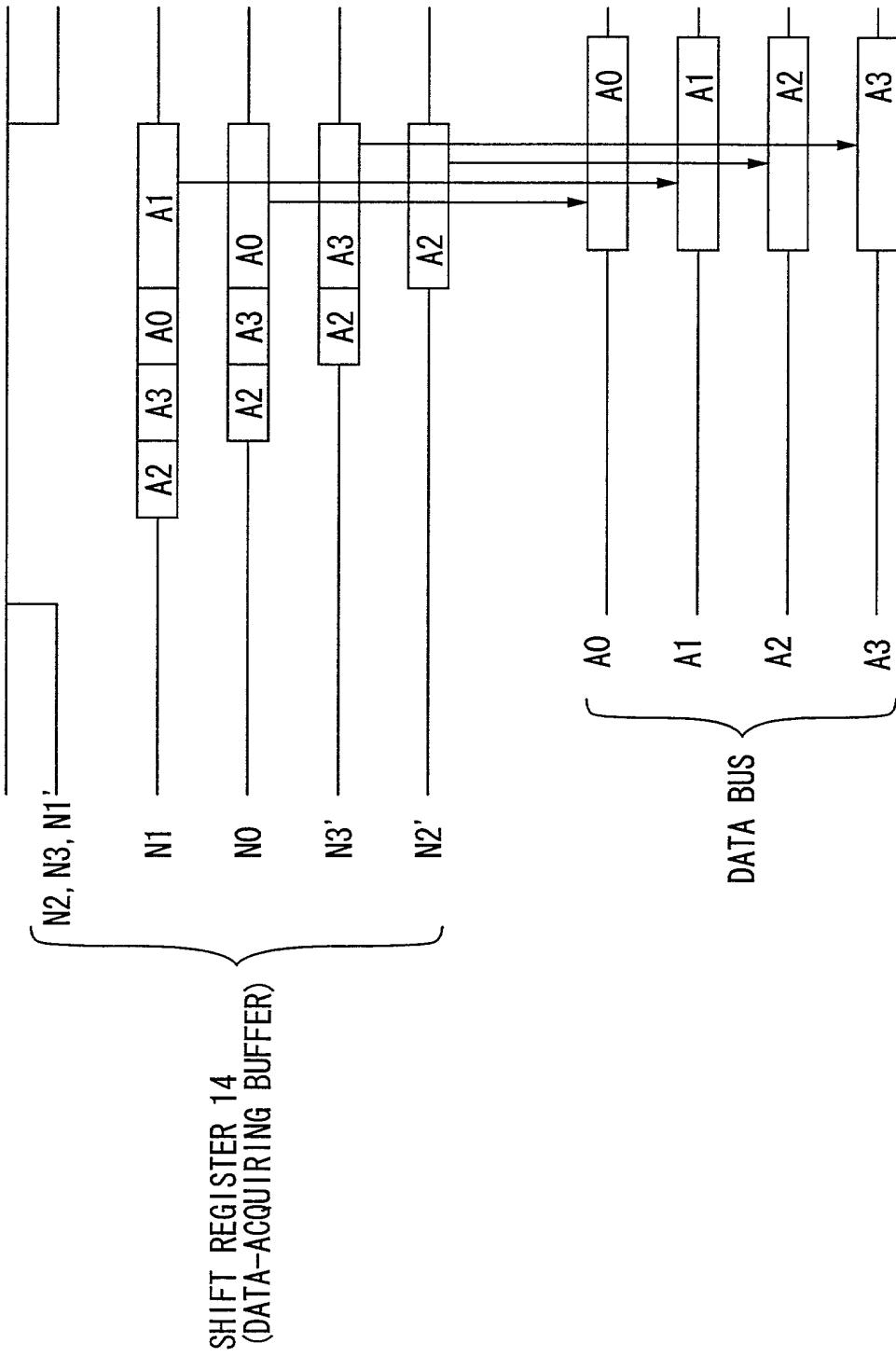


FIG. 7

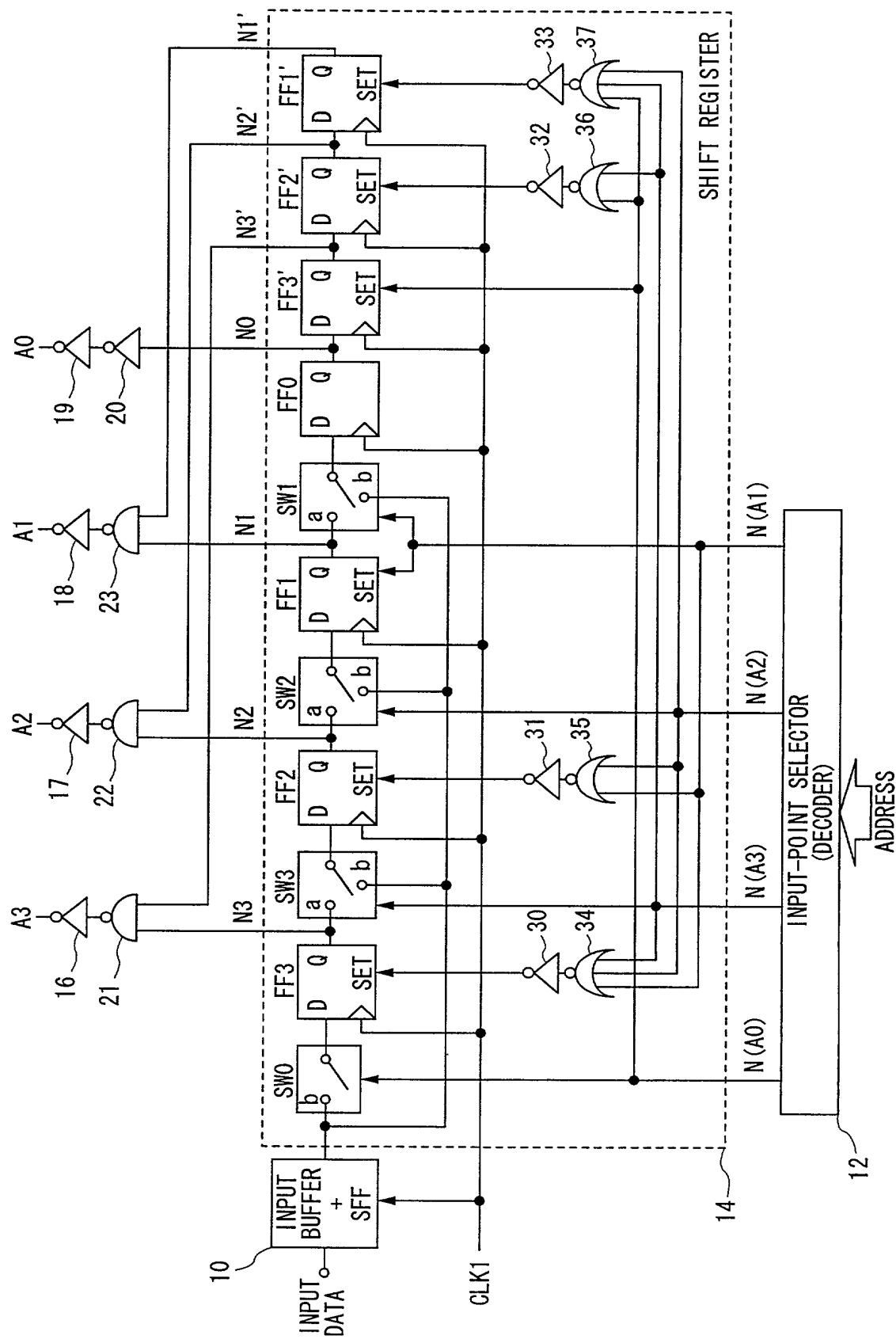


FIG.8

2

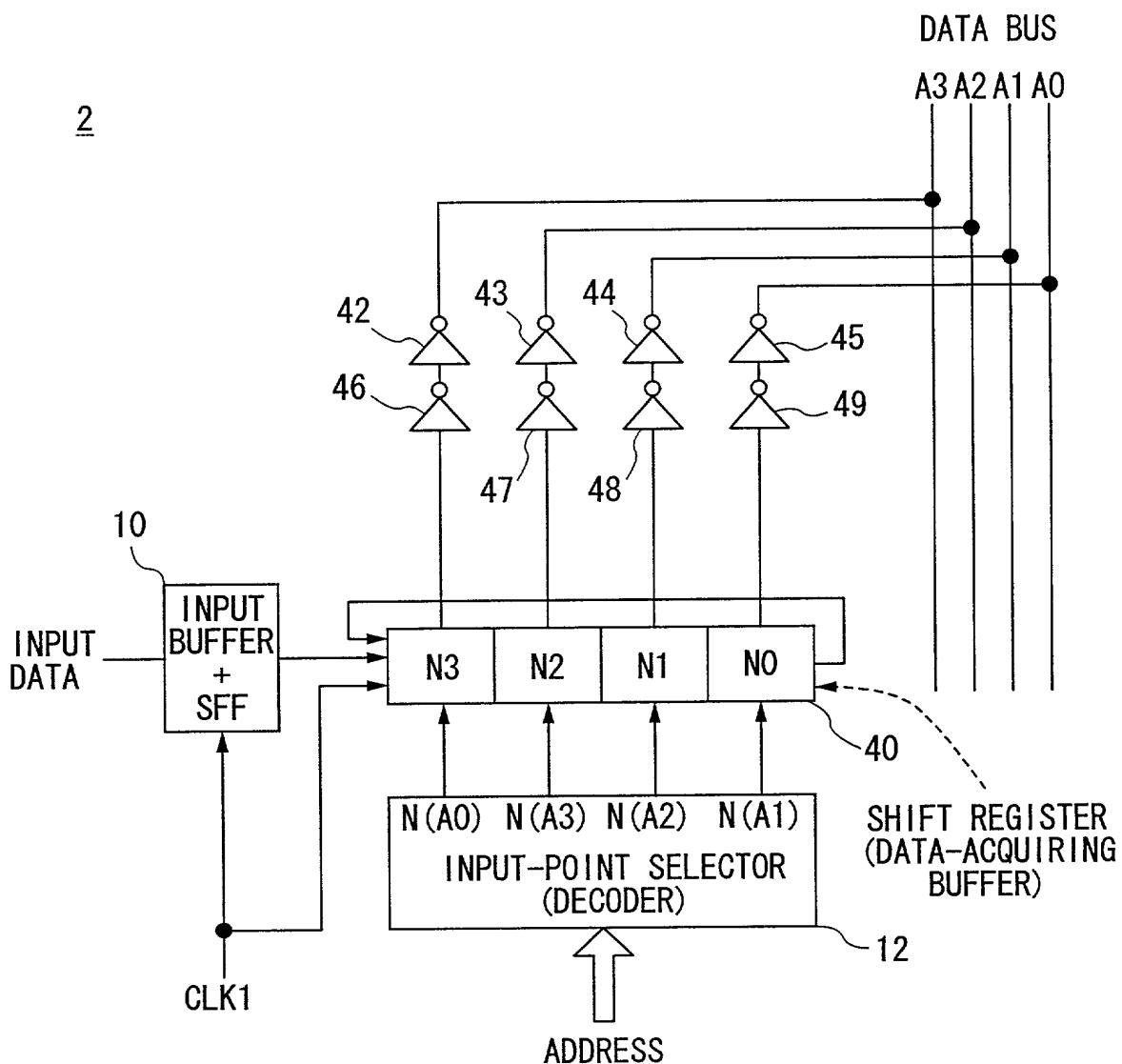
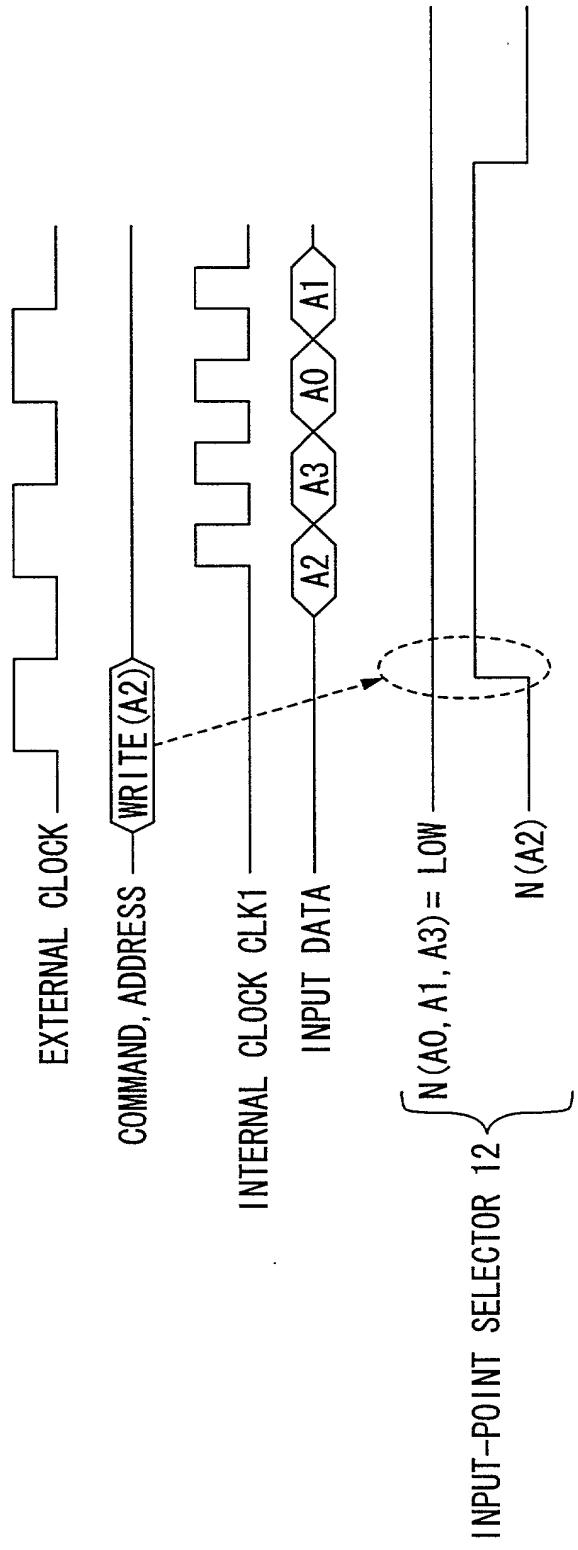


FIG.9A



shift register 40
(data-acquiring buffer)

FIG.9B

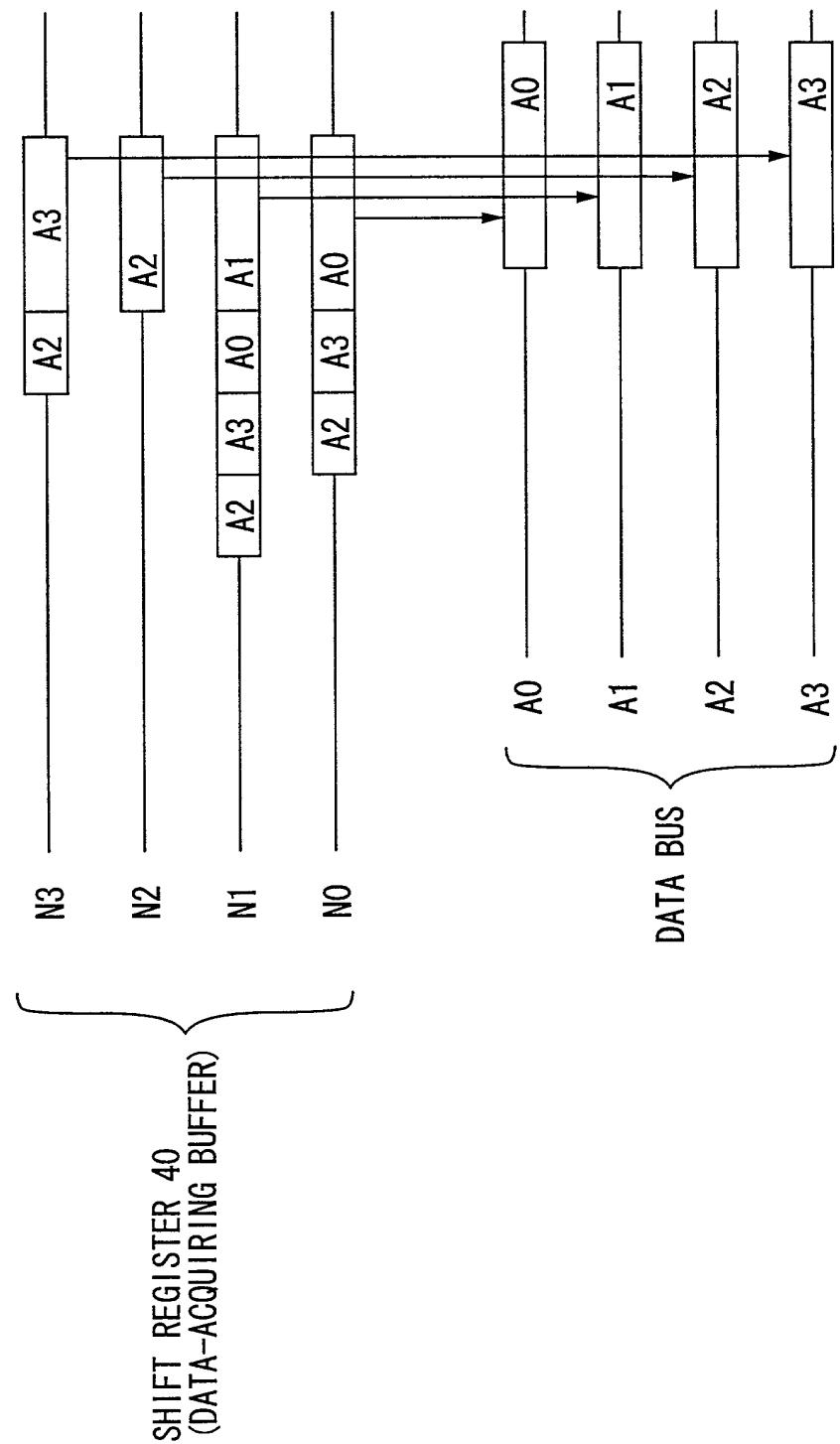


FIG.10

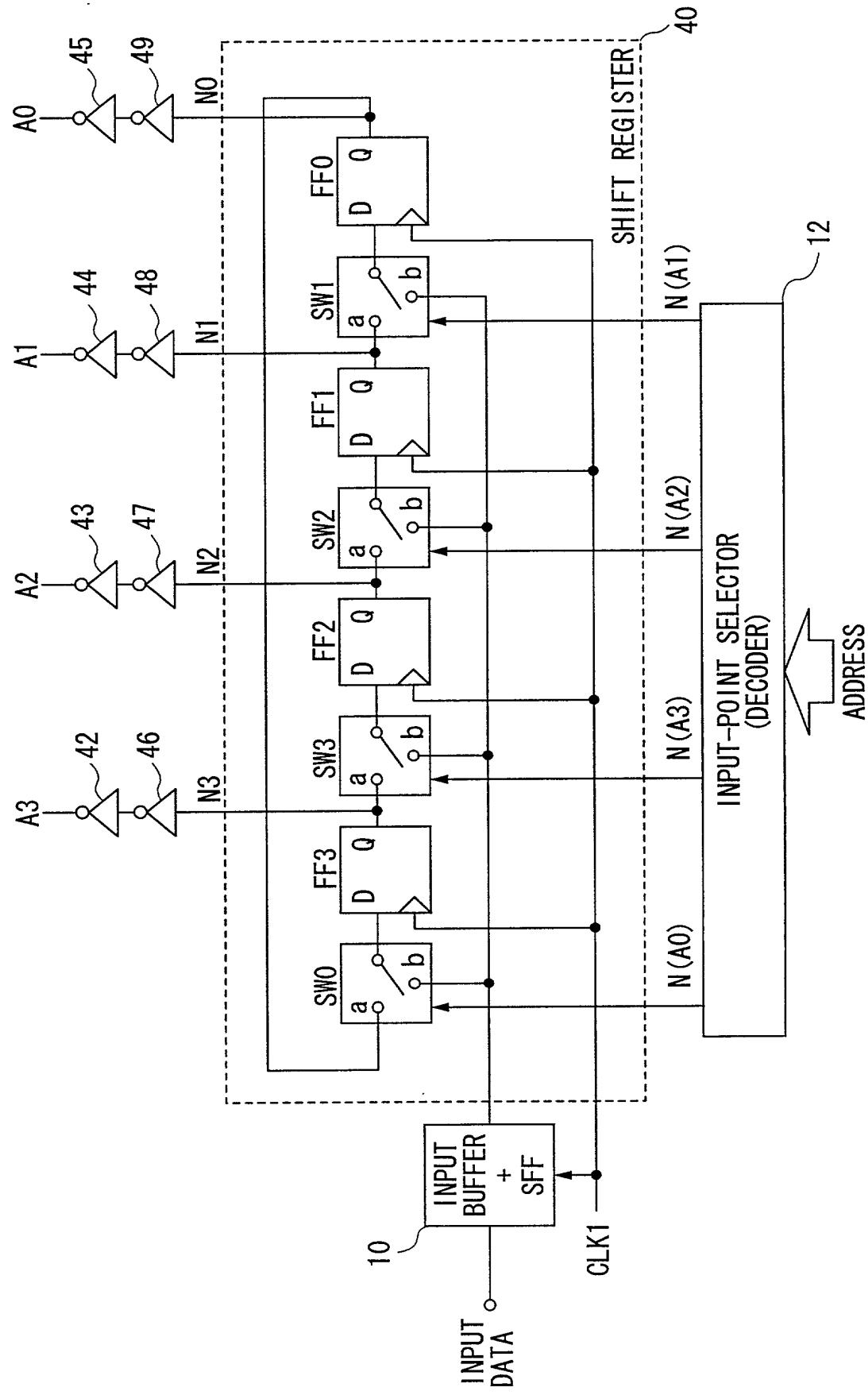


FIG. 11

